Porous Silicon Fabrication Process for Optical Reflectors

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ABSTRACT

We describe the use of porous silicon fabrication technique for fabricating non-manhattan structures in silicon using wet etching. The fabrication method is simple to set up, economical and produces smooth etched surface. A solid source diffusion of N++ in a P type wafer with low stress thermally grown silicon nitride is used as a masking layer. Comparison of porous silicon etches with wafers solid source diffusion and implanted diffusion is presented. The result show that areas where a solid source diffusion is used form an etch angle of 70-80°, however using an implanted diffusion the etch angle is closer to 90°. The selectivity of the etch during porous silicon fabrication using any of the above two as masking layer results in fabrication of high aspect ratio non-manhattan structures. These structures since are wet etched do not have surface roughness and can be used for optical applications.

Keywords: Porous silicon, non-manhattan, high aspect ratio, MEMS, wet etching

INTRODUCTION

Successful implementation of the wet deep etching process would enhance the capabilities of state of the art MEMS processing by a) allowing fabrication of random geometries with high aspect ratio's using wet silicon etching b) drastically reducing the time required to fabricate high aspect ratio structures in silicon using the current state of the art c) reducing the cost of fabricating high aspect ratio structures by several orders of magnitude in comparison to the

current state of the art, not to mention the advantage MEMS designers and fabrication experts will have in developing and manufacturing MEMS devices with the knowledge of the viability of such a technique [1-6]. Currently the technique that is employed to fabricate high aspect ratio structures in silicon is the DRIE. Although this technique has several advantages over conventional wet silicon etching, the costs of machinery and process materials are relatively high. Consequently the cost per wafer increases. The cost of a typical DRIE system with the ability to handle 4 inch wafers is expensive [7-9]. While the cost of processing the wafer using DRIE is based on features being etched and time, the typical cost of etching is economical. Wet etching of Si, commonly employed by the MEMS industry to fabricate membrane based structures and etches not requiring vertical sidewalls, is the preferred technique in the industry. The preference is based on simplicity, cost effective and easy implementation. While this is the preferred etching technique, DRIE has found acceptance in the etching process because of the limitations of conventional wet etching, such as (a) the formation of a 54.7 degree sidewall angle while etching high aspect ratio structures in <100> type silicon, (b) very long etching times at elevated temperatures and (c) the limitation in achievable aspect ratio. Thus a need exists to develop and implement a wet etch technique that can produce high aspect ratio structures, like DRIE, employing a simple set up, that has minimal operating costs and, in a short period of time.

DEEP WET ETCHING (DWE)

DWE is an alternative approach to DRIE and conventional wet etching. Our research exploited an alternate form of silicon etching namely the porous silicon etching technique, coupled with post processing techniques, to achieve high aspect ratio structures. The unique aspect of this

research is the demonstrated process control that we can exercise on the etching process, to control the shape and morphology of meso-pores of Si. While porous silicon etching has been an active area of contemporary research, most of the research efforts are focused on development of sensor applications [9, 10] or understanding the mechanisms of the process [5, 11-13]. The etched structures of this process are pores of Si of various diameters and shapes which can be modified by controlling various etch parameters and variables such as the applied voltage, current density, etchant concentration, etch time, wafer type etc. Some attempts have been made in the past to create high aspect ratio through wafer structures by using the porous silicon technique through filling the pores with polysilicon, patterning and etching polysilicon and dissolving the pores [3, 8, 10, 12]. While achieving modest success, this techniques was still very time consuming and required numerous pre and post processing steps. Also, the walls of the resulting structures were scalloped due to the partially undissolved pores at the edge of the structures and the definition of the overall feature was compromised [4, 6, 10, 12].

DWE has its advantages of high aspect ratio in Silicon with side wall angles very close to 90 degrees, by controlled mesoporous Si etching. The principle of this technique is to effectively localize the pore formation phenomenon only in desired regions of the wafer. Our initial experiments confirm that it can achieved by masking the areas where etching is not desired with a mask and subjecting the wafer to porous silicon etching in a standard set up. This results in the unmasked area being etched with pores with average diameters of 40 nm. These pores are subsequently dissolved in a wet chemical etchant such as Tetra Methyl Ammonium Hydroxide (TMAH) or Potassium Hydroxide (KOH) at room temperature. The pore diameter effectively controls the roughness of the surface.

One of the primary challenges of this approach is to confine pore formation only to those areas of the wafer where etching is desired. We developed a combined optical/electrical pumping process with process control to control the region of nanopore growth. Another challenge is to maintain the vertical profile of the pores by optimizing the current density, applied voltage, etchant concentration [1, 2]. Pore branching can also compromise the definition of the desired structure, these issues are discussed in detail later. Although a nitride mask effectively stops pore formation, it is undercut there is considerable undercutting due to the presence of native oxide film prior to sputtering of the nitride film. The oxide film is attacked by the Hydrofluoric Acid solution and over the period of etching time erodes it away creating a liftoff of the nitride film. One possible way of overcoming this problem is to use epitaxially grown silicon nitride or chemical vapor deposited (CVD) nitride instead of sputtered nitride.

EXPERIMENTAL RESULT

Ideally the pores should grow vertically into the bulk of the silicon starting from the surface. If the current densities are not maintained at the appropriate levels the pores might branch leading to an ill-defined final structure as seen in figure 1. Also, higher applied voltages and currents can lead to considerable pore branching.

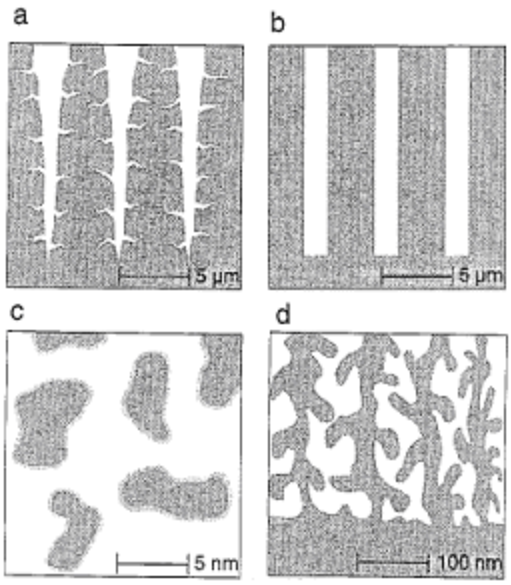
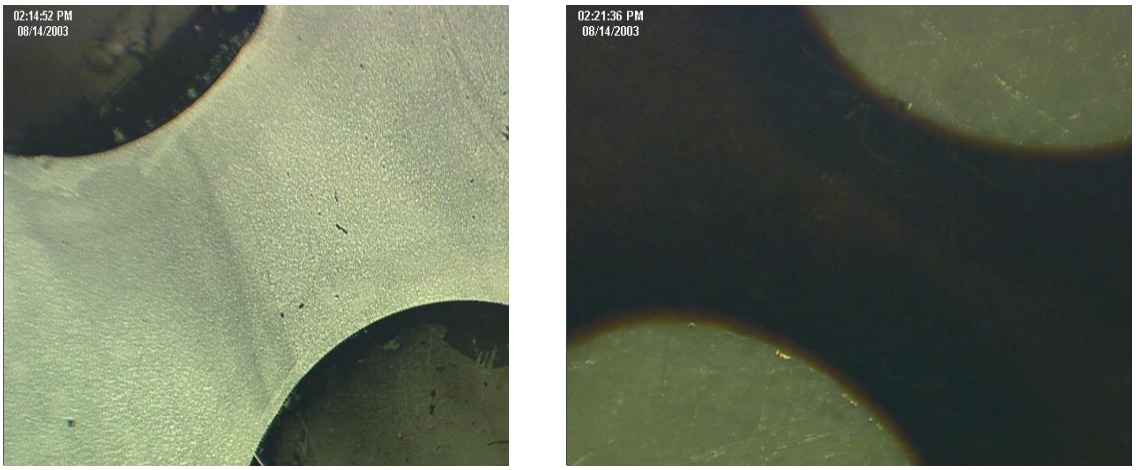


Figure1: Effects of variations in etch parameters on pore geometry

There are two variations of this technique based on the nature of the pores and the usage of light during pore formation namely, macropores and nanopores (these are also called micropores in some literature, we refer to pores which has dimensions in nano scales as nano pores). In the macro porous etching, the pores are orderly and are initiated by KOH etch pits formed by lithography. Backside wafer illumination is also used to help the progression of etching in an anisotropic fashion. In the case of nano porous silicon light activation and pore initiation are not employed and the pores are random in nature with diameters in the nanometer range. We exploited the nano porous silicon formation in this research to achieve high aspect ratio structures, by dissolving these pores in standard silicon chemical etchants. The rate of porous silicon formation depends on a variety of factors such as HF concentration, applied current density, and dopant type/concentration. Due to the dependence on holes for porous silicon formation, there exists a difference in the mechanism by which pores are formed in an N-type and a P-type substrate. P-type silicon which is rich in holes develops pores at any

concentration, whereas N-type silicon in which holes are minority carriers requires some form of hole generation mechanism. Typically a light source is used to pump photons into the substrate for hole generation in N-type silicon for pore formation.



(a) (b)

Figure 2 (a) Micro photographs of circular shapes etched for porous silicon. (b) Substrate after pore dissolution.

As seen from figure 2, on the right the pattern has porous silicon in selective area. N-type silicon can be employed in a P-type substrate as an etch stop layer for pore formation and pore formation is significantly reduced while progressing from an N-type area to a P-type region. To establish the feasibility of this research experiments were carried out to a) localize the porous silicon formation to only certain regions of the wafer b) achieve a highly anisotropic, minimally branched pore profile c) maintain the straightness of the overall structure walls. Traditional porous silicon processing involves forming pores throughout the surface of the wafer. Previous work has been reported in literature regarding localizing pores , but this is confined to shallow structures which are not very deep. We have successfully been able to localize pores only in the

regions of interest and prevent pore formation in the rest of the wafer by using a combination of etch masks.

CONCLUSION

We were able to fabricate nanopores selectively using a p type silicon wafer and the pattern was defined using silicon nitride as the masking layer and forming the least resistance path for the areas where nanopores are to be formed. Nanopores were formed and they were then etched using anisotropic etchant to etch away the nanopores silicon quickly at room temperature. This allows us to make optical quality surface useful for optical application. This process is not only cost effective but also provides a smoother surface which are the two major advantage of this process.

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